UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,249	02/25/2004	John A. Hayden	A0312.70515US00	2715

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EXAMINER
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2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)
	10/786,249	HAYDEN, JOHN A.
	Examiner	Art Unit
	Jasjit S. Vidwan	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>29 October 2007</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-8,25 and 27</u> is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-8 & 25, 27</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☐ All b)☐ Some * c)☐ None of:

  1.☐ Certified copies of the priority documents have been received.

  2.☐ Certified copies of the priority documents have been received in Application No. _____.

  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
  Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see remarks, filed 10/29/07, with respect to the rejection(s) of claim(s) 1 under Heath have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Heath and further in view of Dowling.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-3, 7, 25 & 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Heath et al, U.S. Patent No: 4,901,234 **[herein after Heath]** and further in view of Dowling, U.S. Patent No: 6,163,836 **[herein after Dowling]**.

1. **As per Claim 1**, Heath teaches DMA controller **[Fig. 1, element 12]** comprising:

> (a) At least one peripheral DMA channel for handling DMA transfers on a peripheral access bus **[Col. 2, Lines 34-41** – *Some peripheral devices are assigned their own DMA channels while others share remaining DMA channels***]**

> (b) At least one memory DMA stream **[see Fig. 1, connection between element 12 (DMA controller) and 15 (Main Memory) & also between element 17 (Aux. Memory) and DMA controller** – *memory DMA stream being address/data transfer between the DMA controller and memory*], including a memory destination channel and a memory source channel **[Col. 3, Lines 47-55** – *Multiple channels for plurality of peripherals including memory*] for handling DMA transfers on first **[Fig. 1, element 26, *"System bus"*]** and second memory access buses **[Fig. 1, element 25, *"Family bus"*]**

(d) First and second memory pipelines for supplying memory addresses **[Fig. 4, Element**

"Address Bus"] to the first **[Fig. 1, element 26, "System Bus"]** and second memory

access buses **[Fig. 1, element 25, "Family Bus"]**, respectively, and for transferring data

on the first and second memory access buses **[Col. 3, Lines 21-32]**

Heath teaches above teachings, however fails to disclose a controller having first and second

address computation units for generating addresses at the same time to permit DMA transfer of data.

Dowling teaches the above deficiency by teaching a controller **[see Dowling, Fig. 2, element 200]**

comprising:

(c) First and second address computation units **[see Dowling, Fig. 2, element 212 &**

106] for computing updated memory address for DMA transfer **[Col. 6, Lines 27-44]** wherein the first and

second address computation units generate addresses at the same time **[Col. 20, Lines 25-30 – Both**

AAU will provide addresses on the same clock cycle edges] to permit DMA transfer of data from one

memory space to another memory space on the first and second memory access buses.

(d) A multiplexer configured to supply first and second current memory addresses to

selected ones of the first and second memory pipelines in response to control signal **[see Fig. 2, element**

122].

It would be obvious to combine the two teachings above in order to take advantage of providing

the controller with versatility in having not only a fixed address computation unit but also a

customizable/programmable address computation unit alongside for providing more efficient processing

means. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would

have been motivated to combine the two teachings.

2.   **As per Claim 2**, Heath as modified by Dowling teaches a DMA controller further comprising a

peripheral prioritizer **[see Fig. 1, element 11, "Central Arbitration control circuit"]** for prioritizing DMA

requests for access to the peripheral access bus and a memory prioritizer for prioritizing DMA requests

for access to one or both of the memory access buses **[Col. 5, Line 65 – Col. 6, Line 2]**

3.   **As per Claim 3**, Heath as modified by Dowling teaches a DMA controller further comprising a traffic controller **[Fig. 3, element 72]** configured to give preference to consecutive transfers in one direction on one or more of the buses **[Col. 3, Lines 61-68]**

4.   **As per Claim 7**, Heath as modified by Dowling teaches a DMA controller wherein the multiplexer is configured to receive the first current memory address from one of the peripheral DMA channels or one of the memory destination channels **[Col. 3, Lines 47-55]** and to receive the second current memory address from one of the memory source channels and to supply the first and second current memory addresses to selected ones of the memory pipelines **[Col. 4, Lines 33-38]**.

5.   **As per Claim 25**, Heath as modified by Dowling teaches a DMA controller **[Fig. 1, element 12]** wherein the controller is programmable to transfer data from the peripheral access bus through the at least one peripheral DMA channel and one of the memory pipelines to one of the memory access buses, to transfer data from one of the memory access buses through one of the memory pipelines and that at least one peripheral DMA channel to the peripheral access bus and to transfer data from one memory location to another memory location, through the memory source channel and the memory destination channel, between the first and second memory access buses **[Col. 3, Lines 21-32]**.

6.   **As per Claim 27**, Heath as modified by Dowling teaches a DMA controller wherein the multiplexer supplies the first and second current memory address to the first and second memory pipelines at the same time **[Col. 5, Lines 13-20]**

7.   Claims 4-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heath and Dowling further in view of Bowes et al, U.S. Patent No: 5,655,151 **[herein after Bowes]**.

8.   **As per Claim 4**, Heath teaches the limitations of Claim 1, however does not disclose the specific structure of the plurality of channels, therefore fails to teach a DMA controller wherein each of the peripheral DMA channels has a data FIFO with inputs receiving data from the peripheral access bus and the memory access buses and with outputs supplying data to the peripheral access bus and the memory access buses.

However, Bowes teaches, in an analogous apparatus and method, a DMA controller **[Fig. 2A, element 218]** wherein each peripheral DMA channel **[Fig. 2B, element 244,** *"Multiple DMA channels"***]** has a data FIFO **[see Fig. 3, element 310]** with inputs receiving data from the peripheral access bus and the memory access buses **[see Fig. 2B & 3, element 261** – *Inputs from peripheral I/O controllers*] and with outputs supplying data to the peripheral access bus and the memory access bus **[see Fig. 3, element 264 & 268]**.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify the system of Heath with the above teaches of Bowes. One of ordinary skill would have been motivated to make such modification in order to program additional DMA transfers before the currently active transfer has been completed increasing system efficiency as suggested by Bowes **[see Col. 3, Lines 13-25]**

9.   **As per Claim 5**, Heath as modified by Bowes teaches a DMA controller further comprising an urgent controller **[see Bowes, Fig. 2b, element 250]** configured to increase the priority of a memory transfer when a peripheral DMA request is received and the data FIFO in a corresponding peripheral DMA channel is not ready to transfer data **[see Bowes Col. 3, Lines 15-21]**

10.   **As per Claim 6**, Heath as modified by Bowes teaches a DMA controller wherein each of the one or more memory destination channels **[See Fig. 3, element 244]** has a data FIFO with inputs receiving data from the memory access buses and outputs supplying data to the memory access buses **[see Fig. 3, element 310]**

11.   **As per Claim 8**, Heath as modified by Bowes teaches a DMA controller **[see Heath, Fig. 1, element 12]** wherein each of the memory pipelines **[see Heath, Fig. 1, element 25 & 26,** *"System bus"* **&** *"Family Bus"***]** includes an address **[see Heath, Fig. 4, "Address bus"]** and write data pipelines for supplying memory addresses and write data to the respective buses **[see Bowes, Fig. 3, element 320]**, a read data pipeline for receiving read data from the respective buses and a control flow pipelines for controlling the flow of control information during a memory access **[Fig. 3, element 330]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
11/26/07

ALFORD KINDRED
SUPERVISORY PATENT EXAMINER